Customer No.: 31561
Application No.: 10/064,424
Docket No.: 9407-US-PA

AMENDMENT

Please amend the application as indicated hereafter.

In the Claims :

1. (original) A laminated substrate structure, wherein the structure comprises a plurality of dielectric layers and a plurality of circuit layers stacked with each other, each of the dielectric layers has a plurality of via studs, and the circuit layers are electrically coupled with each other through the via studs, the laminated substrate structure is characterized by a pattern of circuit layers designed as landless.

2. (original) The laminated substrate structure of claim 1, further comprising at least a via opening layer, arranged on the two most exterior dielectric layers of the dielectric layers.

3. (original) The laminated substrate structure of claim 1, wherein the via opening layer is a dielectric layer, and the dielectric layer has a plurality of openings.

4. (original) The laminated substrate structure of claim 1, whether the via opening layer is a solder mask layer, and the solder mask layer has a plurality of openings.

5. (original) A laminated substrate structure, comprising:

a plurality of dielectric layers, each of the dielectric layers has a plurality of via studs; and

a plurality of circuit layers, arranged in between the dielectric layers, the circuit layers are electrically coupled to each other through the via holes, wherein the via holes in the two most exterior dielectric layers are used as a plurality of solder pads directly.

6. (original) The laminated substrate structure of claim 5, wherein a pattern of the circuit layers is designed as landless.

7. (original) The laminated substrate structure of claim 5, further comprising at least a via opening layer, arranged on the two most exterior dielectric layers of the dielectric layers.

8. (original) The laminated substrate structure of claim 7, wherein the via opening layer is a dielectric layer, and the dielectric layer has a plurality of openings.

9. (original) The laminated substrate structure of claim 7, whether the via opening layer is a solder mask layer, and the solder mask layer has a plurality of openings.

10. (canceled) A laminated substrate manufacture method, comprising:

providing a first supporter;

forming a patterned circuit on the first supporter;

forming a first dielectric layer on the first supporter, wherein the patterned circuit is covered by the first dielectric layer to form a dielectric layer having the patterned circuit on the first supporter;

providing a second supporter;

forming a plurality of via studs on the second supporter;

forming a second dielectric layer on the second supporter, wherein the via studs are extruded from the second dielectric layer to form a dielectric layer having the via studs on the second supporter; and

aligning and laminating a plurality of dielectric layers having the patterned circuit and a plurality of dielectric layers having the via studs, so that the via studs penetrate through the first dielectric layer and electrically couple to the patterned circuit.

11. (canceled) The laminated substrate manufacture method of claim 10, wherein after the dielectric layers having the patterned circuit and the dielectric layers having the via holes are aligned and laminated, a curing step is further performed, so that the first dielectric layer and the second dielectric layer are cured and the conductive positions are electrically coupled at the same time.

12. (canceled) The laminated substrate manufacture method of claim 10, wherein the method to form the patterned circuit comprises:

forming a conductive layer on the first supporter;

forming a patterned photoresist on the conductive layer; and

using the patterned photoresist as a mask, removing a portion of the conductive layer that is not covered by the patterned photoresist to form the patterned circuit.

13. (canceled) The laminated substrate manufacture method of claim 10, wherein the method to form the patterned circuit comprises:

forming a first conductive layer on the first supporter;

forming a patterned photoresist on the conductive layer, wherein the patterned photoresist has a plurality of openings;

forming a second conductive layer in the second openings;

removing the patterned photoresist; and

removing the first conductive layer that is not covered by the second conductive layer to form the patterned circuit.

14. (canceled) The laminated substrate manufacture method of claim 10, wherein the first dielectric layer is formed by using a coating method.

15. (canceled) The laminated substrate manufacture method of claim 10, wherein the method to form the via studs comprises:

forming a conductive layer on the second supporter;

forming a patterned photoresist on the conductive layer; and

using the patterned photoresist as a mask, removing a portion of the conductive layer that is not covered by the patterned photoresist to form the via studs.

16. (canceled) The laminated substrate manufacture method of claim 10, wherein the second dielectric layer is formed by using a coating method.

17. (canceled) The laminated substrate manufacture method of claim 10,

wherein the dielectric layers having the patterned circuit and the dielectric layers having the via studs are laminated by using a vacuum thermal lamination method.

18. (canceled) A laminated substrate manufacture method, comprising:

forming a patterned circuit on a first supporter;

forming a first dielectric layer on the first supporter, wherein the patterned circuit is covered by the first dielectric layer to form a dielectric layer having the patterned circuit on the first supporter;

forming a plurality of via studs on a second supporter;

forming a second dielectric layer on the second supporter, wherein the via studs are extruded from the second dielectric layer to form a dielectric layer having the via studs on the second supporter;

providing at least a via opening layer, wherein the via opening layer has a plurality of openings; and

aligning and laminating a plurality of dielectric layers having the patterned circuit, a plurality of dielectric layers having the via stud, and the via opening layer so that the via studs penetrate through the first dielectric layer and electrically couple to the patterned circuit.

19. (canceled) The laminated substrate manufacture method of claim 18, wherein after the dielectric layers having the patterned circuit, the dielectric layers having the via holes, and the via opening layer are aligned and laminated, a curing step is further performed, so that the first dielectric layer and the second dielectric

layer are cured and the conductive positions are electrically coupled at the same time.

20. (canceled) The laminated substrate manufacture method of claim 18, wherein the method to form the patterned circuit comprises:

forming a conductive layer on the first supporter;

forming a patterned photoresist on the conductive layer; and

using the patterned photoresist as a mask, removing a portion of the conductive layer that is not covered by the patterned photoresist to form the patterned circuit.

21. (canceled) The laminated substrate manufacture method of claim 18, wherein the method to form the patterned circuit comprises:

forming a first conductive layer on the first supporter;

forming a patterned photoresist on the conductive layer, wherein the patterned photoresist has a plurality of openings;

forming a second conductive layer in the second openings;

removing the patterned photoresist; and

removing the first conductive layer that is not covered by the second conductive layer to form the patterned circuit.

22. (canceled) The laminated substrate manufacture method of claim 18, wherein the first dielectric layer is formed by using a coating method.

23. (canceled) The laminated substrate manufacture method of claim 18,

wherein the method to form the via studs comprises:

forming a conductive layer on the second supporter;

forming a patterned photoresist on the conductive layer; and

using the patterned photoresist as a mask, removing a portion of the conductive layer that is not covered by the patterned photoresist to form the via studs.

24. (canceled) The laminated substrate manufacture method of claim 18, wherein the second dielectric layer is formed by using a coating method.

25. (canceled) The laminated substrate manufacture method of claim 18, wherein the dielectric layers having the patterned circuit, the dielectric layers having the via studs, and the via opening layer are laminated by using a vacuum thermal lamination method.

26. (canceled) The laminated substrate manufacture method of claim 18, wherein the methods to form the openings comprise mechanical drilling, laser drilling, and punch.

27. (canceled)A laminated substrate manufacturing process, comprising steps of:

forming a plurality of patterned circuit parts;

forming a plurality of via stud parts;

forming a plurality of via opening parts; and

laminating the patterned circuit parts, the vis stud parts amd the via opening

parts to complete the laminated substrate.